Research article

ESTIMATION OF ACCURACY LEVELS USING MULTILEVEL CONDITIONAL PROBABILITY BOOTH MULTIPLIER

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ABSTRACT: This paper determines about reducing truncation error that enters into fixed width Booth multiplier designs. Fixed width booth multiplier compensates for the Stop error with Multi-level conditional probability Value. The proposed multilevel conditional probability uses all non-zero code to estimate the truncation error and to achieve higher Accuracy levels. Further, the simple and small multilevel conditional probability compensated circuit is proposed. To achieve the proposed multilevel conditional probability booth multipliers low cost high accuracy performance.

1. INTRODUCTION

Multiplication is one of the most consuming field arithmetic operations in high performance circuits. Fixed width multiplier takes n number of inputs and n is the number of outputs produced. Combination of fixed multiplier and multiplier Post stump, cuts half of the LSB produces the result after calculating all the products and gives a high degree of accuracy, but it accepts large circuit area. Direct cut Multiplier fixed-width multiplier cuts half LSBs reduce product directly to circuit area, but it produces truncation error. Compensated circuit has developed in this work to get the balance between accuracy and circuit area.

One way to speed up the multiplication is Booth encoding, which performs the various steps of the multiplication immediately and returns the number of partial products is reduced. It is an efficient algorithm for signed multiplication number, the treated both positive and negative number uniform. It multiplies two signed binary numbers in two's complement. Booth multiplication is a technique that allows small, fast multiplying circuits, the numbers multiplied by transcoding. It is used the standard methods in chip design, and offers significant improvements over the "long multiplication" technology. Most digital signal processing applications are of fixed width multipliers. In this type of multiplier, the length of the input and output bits are the same. Here Half significant parts cutting the error. Error trimmed compensated circuits in this type of multiplier used. Fixed width multiplier produce two types of truncation parts: contribution reduced multiplier, achieve high accuracy that cuts half of the LSB results after calculation of all products and it requires a large circuit area to calculate the cutting part. Direct blunt to save multiplier truncate half of
LSB’s products directly to the circuit area, both produce large truncation error.

In previous adaptive estimator conditional probability was used to improve the accuracy, it uses single non-zero code, the rounding errors during the MLCP procedure that all non-zero code calculation appreciate for cutting error. The compensated circuit is to respond quickly, creates a closed shape with different bit widths L and column information w. Thus accuracy can be adjusted by changing Column information.

2. RELATED WORK

2.1 AREA-EFFECTIVE AND POWER-EFFICIENT FIXED-WIDTH BOOTH MULTIPLIERS USING GENERALIZED PROBABILISTIC ESTIMATION BIAS

A closed form of compensation function for fixed-width Booth multipliers using generalized probabilistic estimation bias (GPEB) is proposed. Based on the probabilistic estimation from the truncation part, the GPEB circuit can be easily built according to the proposed systematic steps. The GPEB fixed-width multipliers with variable-correction outperform the existing compensation circuits in reducing error. An 8x8 GPEB Booth multiplier improves more than 88% on the reduction of absolute average error compared with the traditional direct truncation (D-T) multiplier, and more than 32% area savings is obtained in the GPEB Booth multiplier compared with posttruncation (P-T) Booth multiplier. By the same power consumption, the GPEB Booth multipliers can achieve higher accuracy than the existing works. Besides, considering power efficiency with accuracy, the proposed GPEB Booth multiplier has the most power-efficiency compared with other methods. Furthermore, the GPEB Booth multipliers are implemented in the circuit of two-dimensional discrete cosine transform (DCT). Compared with traditional Booth multiplier’s applications, the proposed 2-D DCT cores can reduce about 18% area cost with the penalty of only 0.8 dB peak signal-to-noise ratio (PSNR). Consequently, the Booth multiplier utilizing area-efficiency, power-efficiency, and high-accuracy is achieved using the proposed GPEB.

2.2 TRUNCATED BINARY MULTIPLIERS WITH VARIABLE CORRECTION AND MINIMUM MEAN SQUARE ERROR

Truncated multipliers compute the most-significant bits of the bits product. This paper focuses on variable-correction truncated multipliers, where some partial-products are discarded, to reduce complexity, and a suitable compensation function is added to partly compensate the introduced error. The optimal compensation function, that minimizes the mean square error, is obtained in this paper in closed-form for the first time. A sub optimal compensation function, best suited for hardware implementation, is introduced. Efficient multipliers implementation based on sub-optimal function is discussed. Proposed truncated multipliers are extensively compared with previously proposed circuits. Experimental results, for a 0.18m technology, are also presented.

2.3 DESIGN OF FIXED-WIDTH MULTIPLIERS WITH LINEAR COMPENSATION FUNCTION

On fixed-width multipliers with linear compensation function by investigating in detail the effect of coefficients quantization. New fixed-width multiplier topologies, with different accuracy versus hardware
complexity trade-off, are obtained by varying the quantization scheme. Two topologies are in particular selected as the most effective ones. The first one is based on a uniform coefficient quantization, while the second topology uses a nonuniform quantization scheme. The novel fixed-width multiplier topologies exhibit better accuracy with respect to previous solutions, close to the theoretical lower bound. The electrical performances of the proposed fixed-width multipliers are compared with previous architectures. It is found that in most of the investigated cases the new topologies are Pareto-optimal regarding the area-accuracy trade-off. We also present experimental results, obtained from a simple multiply-accumulate unit implemented in a 90 nm CMOS technology.

2.4 A HIGH-ACCURACY ADAPTIVE CONDITIONAL-PROBABILITY ESTIMATOR FOR FIXED-WIDTH BOOTH MULTIPLIERS

A single compensation formula of Adaptive conditional-probability estimator (acpe) applied to fixed-width booth multiplier is proposed. Based on the conditional-probability Theory, the acpe can be easily applied to large Length booth multipliers (such as 32-bit or larger) for achieving a Higher accuracy performance. To consider the trade-off between Accuracy and area cost, the acpe provides varying column Information To adjust the accuracy with respect to system Requirements. The 16-bit acpe booth multiplier with Reduces 28.9% silicon area with only 0.39 db signal-to-noise ratio (snr) loss when compared with post-truncated (p-t) booth multiplier. Furthermore, the acpe booth multipliers are applied to Two-dimensional (2-d) discrete cosine transform (dct) to evaluate The system performance. Implemented in a tsmc 0.18 M cmos Process, the dct core with acpe can save 14.3% area .Cost with only 0.48 db peak-signal-to-noise-ratio (psnr) penalty Compared to p-t method.

2.5 A 2.4-GS/S FFT PROCESSOR FOR OFDM-BASED WPAN APPLICATIONS

A fast Fourier transform (FFT) processor that provides high throughput rate (T.R.) by applying the eight-data-path pipelined approach for wireless personal area network applications. The hardware costs, including the power consumption and area, increase due to multiple data paths and increased wordlength along stages. To resolve these issues, a novel simplification method to reduce the hardware cost in multiplication units of the multiple-path FFT approach is proposed. A multidata scaling scheme to reduce wordlengths while preserving the signal-to-quantization-noise ratio is also presented. Using UMC 90-nm 1P9M technology, a 2048-point FFT processor test chip has been designed, and its 128-point FFT kernel has been fabricated for ultrawideband (UWB) applications and also for verification. The 2048-point FFT processor can provide a T.R. of 2.4 GS/s at 300 MHz with a power consumption of 159 mW. Compared with the four-data-path approach, a power consumption saving of about 30% can be achieved under the same T.R. In addition, the 128-point FFT kernel test chip has a measured power consumption of 6.8 mW with a T.R. of 409.6 MS/s at 52 MHz to meet the UWB standard with a saving in power consumption of about 40%.
3. METHODOLOGY:

This system explains about Accuracy Setting fixed width Booth multiplier, uses multi-level conditional probability to Implementation of the compensated circuit. we derive the better error compensation Bias in order to reduce the rounding errors. Then construct a lower error fixed Width Multiplier, the area is for an efficient VLSI implementation.

3.1 MLCP ESTIMATOR

MLCP process creates a closed shape with different bit width L and columns Information w, so that the compensated circuit can be found quickly, and the accuracy can be set column information w. The accuracy is high in MLCP method compared to conditional probability adaptive conditional probability estimator. Although MLCP method has a higher complexity to estimate the truncation Error when compared with adaptive conditional probability estimator.

3.2 FIXED WIDTH BOOTH MULTIPLIER

Modified Booth encoding is popular to reduce the number of partial products. Two L-bit inputs X and Y, and a 2L-bit standard product SP complement representation as follows:

\[ X = X_L2^{L-1} + \sum_{i=0}^{L-2} X_i2^i \]
\[ Y = Y_L2^{L-1} + \sum_{i=0}^{L-2} Y_i2^i \]
\[ SP = X \times Y \]

The modified Booth encoder maps three concatenated inputs y 2i+1, y2i , and y 2i-1, which are tabulated in Table I, where P{y’i}

stands for the probability of y’i. After encoding, there are Q =L/2 rows in the partial product array with an even width L. The corresponding partial products into y’i represented in input xi are tabulated in Table II, where the last column n stands for the sign of each partial product.

<table>
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<tr>
<th>y’i</th>
<th>P_{i0}</th>
<th>P_{i1}</th>
<th>P_{i2}</th>
<th>P_{i3}</th>
<th>P_{i4}</th>
<th>P_{i5}</th>
<th>P_{i6}</th>
<th>P_{i7}</th>
<th>n</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>x_0</td>
<td>x_0</td>
<td>x_0</td>
<td>x_0</td>
<td>x_0</td>
<td>x_0</td>
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<td>x_0</td>
<td>1</td>
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<td>x_3</td>
<td>x_4</td>
<td>x_5</td>
<td>x_6</td>
<td>x_7</td>
<td>x_8</td>
<td>x_9</td>
<td>x_{10}</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>x_0</td>
<td>x_1</td>
<td>x_2</td>
<td>x_3</td>
<td>x_4</td>
<td>x_5</td>
<td>x_6</td>
<td>x_7</td>
<td>0</td>
</tr>
<tr>
<td>-2</td>
<td>x_0</td>
<td>x_1</td>
<td>x_2</td>
<td>x_3</td>
<td>x_4</td>
<td>x_5</td>
<td>x_6</td>
<td>x_7</td>
<td>1</td>
</tr>
</tbody>
</table>

Fixed width Stand encryption algorithm is used mostly in multiplier designs, to reduce the number of the partial products. The partial product array in a cabin Multiplier for induction of the column Information w, where w is the Included Number of true product columns in the compensated circuit.

Architecture of the proposed MLCP Booth Multiplier using ETA array with L=16 and w=3.

3.5 CARRY SAVE ADDER ARRAY
Carry save adder architecture and function of subtracting one is designed by adding all one values for twos complementation representation. The proposed MLCP circuits depend on \( a \), thus, various word lengths \( L \) and column information \( w \) can use the same MLCP circuit.

4. RESULTS AND DISCUSSION

The proposed system provides a comparison of the accuracy, size, power consumption and speed performance.

4.1 ACCURACY

In the architecture described above, we reduce the number of partial product compared. But its the output width is the same as that of the input.

4.2 AREA

The overall equivalent gate count is increased to be increased costs are we to reduce the current consumption and the improvement in speed compared with and by increasing the gate count.

4.3 POWER AND SPEED PERFORMANCE

Hence, reducing the number of partial product so that it consumes low power and great improvement in speed performance.

5. SIMULATION RESULT

5.1 4:2 COMPRESSOR

5.2 BOOTH ENCODER PARTIAL PRODUCT BLOCK
5.3 FULL ADDER

5.4 HALF ADDER

5.5 TP MAJOR

5.6 TP MINOR

6. CONCLUSION
This brief estimates the Stop error with high accuracy using MLCP method compensated with the power of 1.8V. Therefore MLCP circuit can be used to develop a high accuracy, low cost and flexible fixed width Booth multiplier.

7. REFERENCES


