HIGH - SPEED FREQUENCY MULTIPLIER DESIGN FOR DUAL EDGE DETECTOR BASED DLL - CLOCK GENERATOR

V. Ramya¹, M. Vasanthakumar ²

¹ (M.E, Department of Electronics and Communications Engineering, AVS Engineering College, Salem)
Mail id: ramyvasantha10@gmail.com

² (Assistant Professor, Department of Electronics and Communications Engineering, AVS Engineering College, Salem) Mail id: Vassece.win@gmail.com

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ABSTRACT

The aim of delay-locked loop-based clock generator to generate a multiplied clock with a high frequency and wide frequency range. The proposed edge combiner achieves a high-speed and highly reliable operation using a hierarchical structure and an overlap canceller. By applying the logic to the pulse generator and multiplication-ratio control logic design, the frequency of the delay is determined. Finally, a numerical analysis is performed by means of the following frequency multipliers. The multiplication ratios of 1, 2, 4, 8, and 16, and an output range of 100 MHz - 3.3 GHz are from the frequency multiplier is fabricated using a 0.13 μm CMOS process technology. The frequency multiplier achieves power consumption to a frequency ratio of 2.9μW/MHz. The proposed architecture of this paper area and power consumption analysis using tanner tool.

Keywords: DLL, Frequency Multiplier, Edge Combiner.

1. INTRODUCTION

The clock generator is implemented using a phase-locked loop (PLL) to change the output clock frequency. PLLs have several backlogs, as the difficulty of design, expensive loop filters, and accumulation of jitter. The drawbacks of PLL is overcome by Delay-locked loops (DLLs) gives better results to PLLs.; However, because a DLL uses a delay line instead of an oscillator, its output clock frequency is always the same as its input clock frequency. Therefore, a DLL alone cannot be used as a generator of clocks. Many DLL dependant clock generators.

The DLL based clock generator has a DLL and a frequency multiplier, and this frequency multiplier again has two blocks.
To generate different frequencies of different ranges, a controlled logic of multiplication ratio is implemented. The DLL core produces multiphase clocks using a reference clock in the DLL core. The multiphase clocks as per the controlled logic of multiplication, to provide a pulse generator provides the appropriate number of pulses from usually, the maximum multiplication ratio of the frequency multiplier is half of its number of multiphase clocks. Because the frequency multiplier produces the multiplied clock by gathering the multiphase clocks. There will be no jitter accumulation. There can be a variety of multiplication ratios. To have a maximum multiplication ratio, the logic used or output. However, it gradually degrades the maximum multiplied clock frequency. To control the defects of the frequency multiplier used before, a new effective frequency multiplication technique is used in the following paper. A new rearranged structure and canceller of overlapped signal are used in the edge combining process. Here the technique is used in the frequency multiplier. The frequency of the frequency of the multiplied clock by the frequency of the frequency.

Dynamic Voltage Frequency Scaling is currently being used in nearly every System-On-Chip (SoC). Design can be efficiently lower the dynamic power consumption of the SoCs. It detects the SOC workload and dynamically changes the supply voltage and frequency, requires a low power dc converter and a clock generator. The clock generator is used with a phase-locked loop to easily change the output clock frequency. While, PLLs have a number of weaknesses, as is the difficulty of design, high-cost loop filters, and jitter accumulation is high. Delay-locked loops (DLLs) are a good alternative for PLLs, because they are over the PLL drawback however, because a DLL uses a delay line instead of an oscillator, its output clock frequency is always the same as its input clock frequency. Therefore, a DLL alone cannot be used as a clock generator. Several DLL-based clock generators have been designed to solve this problem. The DLL-based clock generator is composed of a DLL core and a frequency multiplier, A Pulse Generator and an Edge Combiner. In case that variable frequency multiplication is required, a multiplication ratio control circuit is added. The DLL core built multiphase clocks using a clock in the DLL core. The pulse generator generates the required number of pulses from the multiphase clocks according to the multiplication-ratio control signal generator,
and the edge combiner generates a multiplied clock using the selected pulses. In general, the maximum multiplication ratio of the frequency multiplier is $N/2$ of the number of multiphase clocks. The multiplied clock by simply collecting the multiphase clocks, jitter accumulation does not occur because of the frequency multiplier generation. In addition, the frequency multiplier can easily change multiplication ratios. The logic depth or output of the frequency multiplier must be increased and the multiplication ratio. However, it severely degrades the maximum multiplied clock frequency.

2. LITERATURE SURVEY

2.1 DLL Based Clock Generator with Low Power and High Speed Frequency Multiplier

Thutivaka Vasudeepthi, P.Malarvezhi and R.Dayana

An effective less power and enhancement of frequency multiplier for a delay-locked loop clock generator is used to produce an increased frequency by multiplied clocks. Here edge combiner whom we have used to enhance multiplied frequency gives more speed and effective operation is done as we use different structure and overlap canceller. On other hand by applying the logic that satisfies our requirement of pulse generator and multiplication-ratio control logic design, we reduces the delay difference between positive- and negative-edge of the generated pulse, which causes a known jitter which we called as deterministic jitter.

2.2 Highly Reliable Frequency Multiplier with DLL-Based Clock Generator for System-On-Chip

B. Janani, N.Arunpriya

High-speed, low-power, fully operational and reliable frequency multiplier is proposed for a delay

Locked loop based clock generator to generate a multiplied clock with a high frequency and maximum frequency range. The proposed edge combiner efficient achieves-speed and highly reliable operation using a hierarchical structure and an overlap deselected. By applying the logical effort to the pulse generator and multiplication-ratio control logic design, the proposed frequency multiplier minimizes the delay difference between positive- and negative-edge generation paths, which causes a measurable jitter. Finally, a jitter analysis is performed to analyze and compare the performance of the proposed frequency multiplier with that of previous frequency multipliers. The proposed frequency multiplier is fabricated using a 2.5-μm technology, and has the multiplication ratios of 20, 21, 22, 23, and
24, and an output range of 50 MHz–3.3 GHz.

2.3 High-Speed, Low-Power, and Highly Reliable Frequency Multiplier for DLL-Based Clock Generator

S. Ghousiya Banu, T. Jenifer, K. Kavitha, Mrs. H. Rashmi Evangelin

A high-speed, low-power, and highly reliable frequency multiplier is proposed for a delay-locked loop-based clock generator to generate a multiplied clock with a high frequency and wide frequency range. The proposed edge combiner achieves a high-speed and highly reliable operation using a hierarchical structure and an overlap canceller. The proposed frequency multiplier minimizes the delay difference between positive-edge and negative-edge generation paths, which causes a deterministic jitter. Finally, a numerical analysis is performed to analyze and compare the performance of the proposed frequency multiplier with that of previous frequency multipliers. The proposed frequency multiplier is fabricated using a 0.13-μm CMOS process technology, and has the multiplication ratios of 1, 2, 4, 8, and 16, and an output range of 100 MHz–3.3 GHz. The frequency multiplier achieves power consumption to a frequency ratio of 2.9 μW/MHz.

2.4 A Low-Power and High-Speed Frequency Multiplier for DLL-Based Clock Generator

Priyadharshini M, Paul Richardson Gnanaraj J

A low-power and high-speed frequency multiplier for a delay-locked loop-based clock generator is proposed to generate a multiplied clock with different range of frequencies. The modified edge combiner consumes low power and achieves a high-speed operation. The proposed frequency multiplier overcomes a deterministic jitter problem by reducing the delay difference between positive- and negative-edge generation paths. The proposed frequency multiplier is implemented in a 0.13-μm CMOS process technology achieved power consumption to a frequency ratio of 2.9 μW/MHz, and has the multiplication ratios of 16, and an output range of 100 MHz–3.3 GHz.

3. EXISTING SYSTEM

The structures of the recently published frequency multipliers that perform better than most previous frequency multipliers. The frequency multiplier is composed of a D-flip–flop-based pulse generator, multiplication-ratio control logic, and a push–pull-stage based edge combiner, as shown in Fig. 1(a). Owing to its simple
edge-combiner structure, this frequency multiplier is suitable for high-frequency multiplied clock generation with low power and a small area. The structure of another frequency multiplier. This frequency multiplier is composed of multiplication-ratio control logic, an AND-gate-based pulse generator, and a differential cascade voltage switch (SW) logic (DCVSL)-stage-based edge combiner. The frequency multiplier can generate the multiplied differential clocks with a small area penalty.

Disadvantages
- Speed is less

4. PROPOSED SYSTEM
The proposed DLL-based clock generator is composed of a DLL core and the proposed frequency multiplier. To achieve the best performance of the device, a dual-edge-triggered phase-detector-based DLL core is adopted. Similar to previous frequency multipliers, the proposed frequency multiplier is also composed of a pulse generator, multiplication-ratio control logic, and an edge combiner. The two-step edge combiner, recombining, and push–pull stage are used to enhance the maximum multiplied clock frequency. The frequency multiplier is the stable operation due to the overlap canceller.

Fig.4.1 Structure of the proposed clock generator
The proposed pulse generator and the multiplication-ratio control logic. These two structures have an optimized design to match the delay between the positive- and negative-edge generation paths of the multiplied clock.

The Delay Lock Loop is locked within (300) three Hundred clock cycles in all process–voltage–temperature corners owing to the dual-edge detection characteristic, and generates 32-phase differential clocks phase 20 to 25 and phase 20 to 25. Using the 32-phase differential clocks, the pulse generator makes pulses Phase G 20:25 and Phase G 20 to 25 for positive- and negative-edge generation. The multiplication-ratio control logic selects appropriate pulses from Phase-G 0:31 and Phase-G 0:31 and generates MC-P, 0:15 and MC-N, 0:15 according to the
multiplication ratio control signal. Finally, the high-speed and highly reliable edge combiner generates one multiplied clock using all the outputs of the multiplication ratio control logic. Hence the number of multiphase is 20 to 25; the maximum multiplication ratio is 16.

5. DESIGN AND IMPLEMENTATION

The signals are merged in the pre-composing stage (NPRE), the number of PU-Ps and PD-Ns are required in the push-pull stage. It may appear that, by increasing NPHR, the maximum multiplied clock frequency of the HSHR-EC can be enhanced; However, the number of NAND gates in the pre-combing stage is equal to log2NPRE and 32 (1-1 / NPRE), respectively, a large NPRE causes the pre-combination stage to be vulnerable to process Variation, which in turn could cause a large deterministic jitter. Thus, NPRE is limited to two, which corresponds to a logic depth of one in the HSHR-EC, and NAND and NOR gates. The proposed frequency multiplier may be from pulse overlapping to the multiplication-ratio control logic as is true for the frequency multipliers. To prevent this, an overlap canceller is inserted between the pre-combing and the push-pull stages. At HSHR-EC, it has a pre-composing stage, overlap canceller, and push-pull stage is proposed. The two-step edge combiner, pre-combining, and push-pull stage are used to enhance the maximum multiplied clock frequency. The overlap canceller is used to guarantee the stable operation of the frequency multiplier.

5.1 CLOCK GENERATOR

In synchronizing a circuit’s operation a clock generator produce timing signal. The signal can range from a simple symmetrical square wave to more complex arrangements.

5.2 DELAY LOCKED LOOP

The delay locked loop is a variable delay line whose delay is locked to the duration of the period of a reference clock. A DLL can be used to change the phase of a clock
data output valid timing characteristics of IC.

5.3 EDGE COMBINER

![Fig.5.3 Edge Combiner](image)

An edge combiner can combine the multiple clock phases and act as a programmable frequency multiplier useful in dynamic voltage.

5.4 FREQUENCY MULTIPLIER

![Fig.5.4 Frequency multiplier](image)

A frequency multiplier generates on output signal whose output frequency is a harmonic of its input frequency.

5.5 CHARGE PUMP

![Fig.5.5 Charge pump](image)

A charge pump is used to provide a charge to a capacitive element on a voltage controlled delay line (voltage controlled delay line). Where in the charge is independent of a control voltage step cycle time of the DLL.

6. RESULT AND DISCUSSION

In this paper the system is achieved by a tanner tool in VLSI design.

6.1 Schematic Diagram

![6.1 Schematic Diagram](image)

6.2 Output of DLL operation

![6.2 Output of DLL operation](image)
6.3 WAVEFORM OF FREQUENCY MULTIPLIER
7. CONCLUSION
In this proposed system dual edge detector based DLL - clock generator is designed by using a high speed frequency multiplier. The pulse generator is reduced a delay between the circuit. The proposed HSHC-EC guarantees high-speed operation in edge combiner and overlapped a canceller. It is highly reliable. This system is designed by using a tanner tool.

8. REFERENCE


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