Design of Ultra Low power DET Flip-Flop with Power gating technique

M.Krishnaveni¹, S.A.Sivakumar ²

¹PG scholar, M.E VLSI Design, Department of ECE, Info Institute of Engineering, Coimbatore.
² Assistant Professor, Department of ECE, Info Institute of Engineering, Coimbatore.

brindhakrishna2@gmail.com

Abstract:
The advancement of battery operated designs has abundantly increases the memory elements and registers to be operated in ultra low power. That is the this paper we have proposed a design of CT_C DET flip-flop with power gating technique which is the most efficient power consuming reduction technique. The design of the power gating technique involves the pull-up transistor in the Vdd of the circuit and pull-down transistor in the Gnd terminal. This power gating technique reduces the power consumption by more than 40% than that of the existing design.

Keywords: DET flip flop, low power consumption, power gating

1. Introduction
The advancements in battery powered devices abundantly increasing these days. These increases in the small power consuming devises increase the importance of sub threshold operating devices are most needed to support the battery operated devices. Normally, high-performance chips have high integration density and high clock frequency, which tend to dictate power consumption. Therefore, designs are that can consume less power while maintaining comparable performance. Power consumption in the conventional CMOS digital circuit can be separated into three types of power dissipation [1]: (i) switching power, (ii) short-circuit power, and (iii) leakage power consumption. The switching power represents the power dissipated during the signal transitions when energy is drawn from the power supply to charge-up the device capacitances. Short-circuit power is produced during the moment that both the PMOS network and the NMOS network are simultaneously on in CMOS logic. The MOSFETs in CMOS logic normally will have some non-zero reverse leakage and sub-threshold current, which causes the leakage power consumption. Using pulse generation for double edge-triggered flip-flops requires more transistors to achieve the proper functionality. Many of those transistors are related to the clock signal, which will increase the activity factor α, and cause increased power consumption. So the dual data-path idea was chosen as the targeted implementation scheme. Also transmission gates are used to diminish the undesirable threshold voltage effects that lead to the weak logic signals in pass transistors. Instead of using a loop comprised of two inverters and one transmission gate as the logic keeper, DET-FF only uses an inverter and a PMOS transistor to keep the logic level.

In recent years, a paper introduced a flip-flop called high speed dual-edge triggered modified hybrid latch flip-flop [2] (HSDMLFF) to improve power consumption by reducing precharge capacitance activity factors. Dynamic explicit pulsed triggered flip-flop (DEPFF) [3], SCCER [4] and DDFF [5] are three other flip-flops that will be discussed earlier. In this work, with effective using of C-element, a new pulsed hybrid flip-flop is introduced. It makes use of C-element as a fundamental stage of its structure, which overcomes the draw-back of additional switching activity as such, and achieving improvement from 7.9% to 55.7% in 12.5% data activity as compared to other designs. Note that these improvement values are increased as simulations are performed in process corners. Further-more, speed and layout area of presented scheme are saved about 5% and 12%, respectively. Among state of the art topologies, pulsed latches potentially are well-suited for applications where targeting energy efficiency from moderate to high performance[6]. Generally, a pulsed DET flip-flop works by making its output latch transparent to the input signal after every clock edge for
a short time interval that is sufficient to reliably latch the input value. Power dissipation of these flip-flops is less dependent on input signal transitions in between the clock edges at the cost of increased power dissipation due to clock activity.

This paper is presented in four distinct sections where the existing work was discussed in Section II, and Section III deals with the proposed DET flip flop. The results and analysis of the existing and proposed designs are discussed in the Section IV. The Section V concludes the work and talks about the future work.

2. CONVENTIONAL CONVERTER

Conditional-Toggle CT_C and CTF_C Flip-Flops the novel conditional-toggle CT_C DET flip-flop design is shown in Figure 1. The CT_C flip-flop circuit uses only 20 transistors including transistors for the input, output, and clock buffering. The flip-flop consists of a dynamic C-element at the output and a latch that provides static behavior to the circuit. The distinguishing feature of the CT_C flip-flop is that the state of its latch does not change when the flip-flop’s output switches after a clock transition, which leads to low switching energy dissipation. The circuit for the output C-element is based on the weak-feedback implementation shown in Fig. 1 but with the feedback inverter eliminated. The inputs to it are input D and the signal that mirrors Q in between clock transitions. When D is equal to Q, the C-element keeps its inverted output X at the level of Q. When D is not equal to Q, the Q level at X is kept by the latch.

The latch part of the circuit is responsible for toggling the signal level at X after clock transitions and for keeping it at Q in between clock transitions when D is not equal to Q. The latch part consists of two inverters connected back-to-back and a bi-directional 2-to-1 multiplexer with its output is connected to node X.

The operation of the CT_C flip-flop is illustrated using simulated voltage traces. The clock signal makes the multiplexer alternate between the two ends of the latch A and B after every clock transition. In between clock transitions, the end of the latch that is connected to X is at Q. After a clock transition, the multiplexer switches to the opposite end of the latch, which makes the signal levels at X and Q toggles if D was not equal to Q before the clock edge. If D is equal to Q when the clock edge arrives, it is the latch that toggles its stored value and not node X, because the C-element forces node X to the level of D. Toggling at the output is not done by changing the value stored by the latch but rather by multiplexing to the inverse of it, which achieves low switching activity within the flip-flop[7].

The latch toggles its stored value after a clock edge only when D is equal to Q. Implementation of the CT_C flip-flop presents trade-offs between power dissipation at high and low switching activities and circuit delay. Strong inverters in the latch make the output switching faster with little impact on the switching energy. However, the stronger these inverters are, the more energy it takes to change the state of the latch, i.e., the higher the power dissipation at low switching activity becomes. In the CTF_C flip-flop, a modification of the CT_C flip-flop, that relaxes these trade-offs is shown. During operation nodes A or B is at D while the other is at D. In the CTF_C flip-flop, the strengths of signal levels at these nodes depend not only on transistor sizing but also on D: Whichever node is at D is kept strongly while the other node is kept weakly with always-on transistors.

If at a clock transition D is not equal to Q, node X is multiplexed to a strong D that quickly changes X to D and Q to D. When D is equal to Q, logic level at node X is kept strongly at D by the C-element. The next clock transition multiplexes node X to a weak D which the C-element overpowers quickly.
and at a low energy cost. Thus, CTF_C achieves faster switching compared to CT_C and reduces energy dissipation of idle cycles.

3. PROPOSED SYSTEM

The design is modified by using the efficient power reduction technique that is power gating. This power gating technique is a noteworthy power reduction technique that is involved in reduction of power in the digital ICs. Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling lddq testing. Power gating implementation has additional considerations for timing closure implementation. The following parameters need to be considered and their values carefully chosen for a successful implementation of this methodology.

1. Power gate size: The power gate size must be selected to handle the amount of switching current at any given time. The gate must be bigger such that there is no measurable voltage (IR) drop due to the gate. As a rule of thumb, the gate size is selected to be around 3 times the switching capacitance. Designers can also choose between header (P-MOS) or footer (N-MOS) gate. Usually footer gates tend to be smaller in area for the same switching current. Dynamic power analysis tools can accurately measure the switching current and also predict the size for the power gate.

2. Gate control slew rate: In power gating, this is an important parameter that determines the power gating efficiency. When the slew rate is large, it takes more time to switch off and switch-on the circuit and hence can affect the power gating efficiency. Slew rate is controlled through buffering the gate control signal.

3. Simultaneous switching capacitance: This important constraint refers to the amount of circuit that can be switched simultaneously without affecting the power network integrity. If a large amount of the circuit is switched simultaneously, the resulting "rush current" can compromise the power network integrity. The circuit needs to be switched in stages in order to prevent this.

4. Power gate leakage: Since power gates are made of active transistors, leakage reduction is an important consideration to maximize power savings.

![Figure 3 Power gating technique](image-url)

The basic strategy of power gating is to provide two power modes: a low power mode and an active mode. The goal is to switch and an active mode. The goal is to switch between these modes at the appropriate time and in the appropriate manner to maximize power savings while minimizing the impact to performance. In this paper, we proposed a flip-flop which includes an upper data path responsive to the rising edge of the clock signal and a lower data path responsive to the falling edge of the clock signal, thereby allowing data to be stored on both the rising edge and the falling edge of the clock signal. Moreover, a multiplexer is used to provide data output buffering.
Figure 4 proposed CT_CDET flip-flop with power gating technique

Fig. 4 shows the block diagram of the proposed circuit. In operation, the upper latch passes data to the output buffer in accordance with a clock signal, and the lower latch passes data to the output buffer in accordance with a complementary clock signal.Latch A has a clock input (Clk) which is inverted to its enabling port, as compared to that for latch B. The two data (D) inputs to the latches are from the single D input. The two outputs of latch A and latch B are input to the "1" and "0" inputs of a multiplexer, respectively. The two enabling inputs of latch A and latch B and the select input (sel) of multiplexer are connected to the system clock. When the clock signal Clk is a logical 0, the upper latch A tracks the D input while the lower latch B holds the present state. Output multiplexer selects the output of latch B as the flip-flop state output. When the clock signal Clk is a logical 1, latch A holds the state of the D input and the multiplexer selects this latch's output as the new state of the flip-flop output, causing a state transition. Also, latch B now tracks the D input to acquire the next "new state". The same operation with the roles of latch A and latch B reversed causes a state transition on the falling edge also.

5. SIMULATION RESULTS

The design of various DET flip flops both the conditional-toggle CT_CDET flip-flop and proposed CT_CDET flip-flop with power gating technique are design in the TANNER Tools 13.0. The transistor level schematic of the flip flops design is designed using the s-edit tool and the simulated using the t-spice and w-edit to view the waveform.

Figure 5 output of the Existing conditional-toggle CT_C DET flip flop

As shown in the figure 5 the output of the CT_CD ET flip flop is forming the Flip flop and giving the operation. The design gives the operation of a flip flop and the operation is explained in the previous chapter itself. Likewise the figure 6 shows the Existing conditional-toggle CTF_C DET flip flop and the operation is explained in the previous chapter itself. When the clock signal Clk is a logical 0, the upper latch A tracks the D input while the lower latch B holds the present state. Output multiplexer selects the output of latch B as the flip-flop state output. When the clock signal Clk is a logical 1, latch A holds the state of the D input and the multiplexer selects this latch's output as the new state of the flip-flop output, causing a state transition. Also, latch B now tracks the D input to acquire the next "new state".

The output of the proposed CT_CDET flip-flop with power gating technique is shown in the figure and the operation is explained in the previous chapter. By the figure 7 it is clear that the output of the proposed CT_CDET flip-flop is more efficient and accurate that of the existing.

One of the features of the LG_C flip-flop is its immunity to overlap between CK and CK signals. A change at the flip-flop’s output is triggered by a change at one of A or B which happens due to a signal transition in either CK or CK respectively. That is, every change at the output is triggered by a transition in only one of CK and CK signals, not both. Thus, although clock overlap has an impact on the timing of output transitions, it cannot cause the flip-flop to fail in latching a correct value. While there are many implementations of C-elements that can be used in the LG_C flip-flop is in the proposed design.
Figure 6: Output of the Existing conditional-toggl
CTF C DET flip-flop

Figure 7: The output of the proposed CT_CDET flip-fo
 flop with power gating technique

Tabulation I: Comparison of the existing and proposed design

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Existing CT_C DET Flip flop</th>
<th>Proposed CT_C DET Flip flop</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFETs</td>
<td>20</td>
<td>24</td>
</tr>
<tr>
<td>Total Nodes</td>
<td>13</td>
<td>17</td>
</tr>
<tr>
<td>Average Power Consumpition</td>
<td>8.671685e-005 watts</td>
<td>1.841334e-007 watts</td>
</tr>
</tbody>
</table>

Figure 8: MOSFETs used

Figure 9: Number of nodes used

Figure 10: Power consumption
The power comparison of the existing and proposed design is listed in the tabulation given in the table 1. From the table it is clear that the proposed flip-flop design is very much less than that of the existing designs.

6. CONCLUSION
In this paper we have proposed a design of CT_C DET flip-flop with power gating technique which is the most efficient power consuming reduction technique. The design of the power gating technique involves the pull-up transistor in the Vdd of the circuit and pull-down transistor in the Gnd terminal. This power gating technique reduces the power consumption by more than 40% than that of the existing design. In future the flip-flop can be used in a memory design or some other flip-flop applications such as LFSR, counters, etc.

References